

# 8K-bit TTL bipolar PROM (2024x4)

# 82S185/185A/185B

## FEATURES

- Address access time: 55ns max
- Input loading: -150µA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One chip enable input
- Outputs: 3-State

## APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

## DESCRIPTION

The 82S185 is field-programmable, which means that custom patterns are immediately available by following the Philips Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and one chip enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

## ORDERING INFORMATION

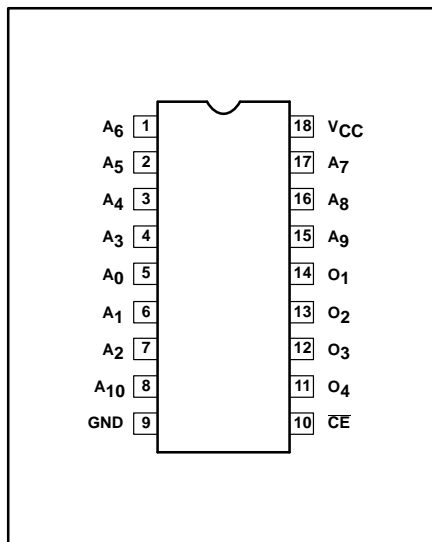
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
18-pin Ceramic DIP (300mil-wide)	82S185/BVA 82S185A/BVA 82S185B/BVA	GDIP1-T18
18-pin Ceramic Flat Pack	82S185/BYA 82S185A/BYA 82S185B/BYA	GDFFP2-F18

\* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

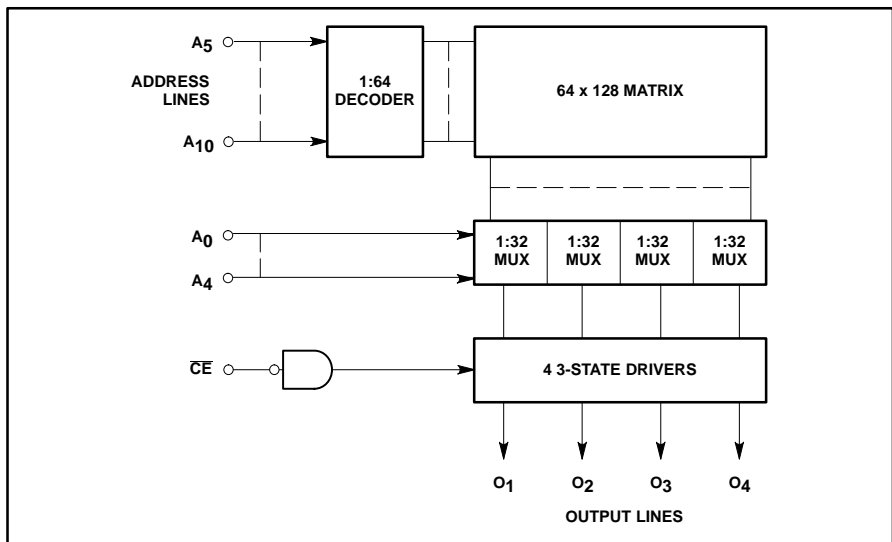
## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	+7	V <sub>DC</sub>
V <sub>I</sub>	Input voltage	+5.5	V <sub>DC</sub>
V <sub>O</sub>	Output voltage Off-State	+5.5	V <sub>DC</sub>
T <sub>A</sub>	Operating temperature range	-55 to +125	°C
T <sub>STG</sub>	Storage temperature range	-65 to +150	°C

## PIN CONFIGURATION



## BLOCK DIAGRAM



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## DC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1, 2</sup>	LIMITS			UNIT		
			Min	Typ <sup>5</sup>	Max			
<b>Input voltage</b>								
$V_{IL}$	Low	$V_{CC} = 4.5\text{V}$ , $I_I = -18\text{mA}$	2.0		0.8	V		
$V_{IH}$	High							
$V_{IK}$	Clamp						-0.8	-1.2
<b>Output voltage</b>								
$V_{OL}$	Low	$V_{CC} = 4.5\text{V}$ , $\overline{CE} = \text{Low}$ $I_O = 16\text{mA}$ $I_O = -2\text{mA}$	2.4		0.5	V		
$V_{OH}$	High							
<b>Input current</b>								
$I_{IL}$	Low	$V_{CC} = 5.5\text{V}$ $V_I = 0.45\text{V}$ $V_I = 5.5\text{V}$			-150	$\mu\text{A}$		
$I_{IH}$	High						40	$\mu\text{A}$
<b>Output current</b>								
$I_{OZ}$	Hi-Z state	$V_{CC} = 5.5\text{V}$ $\overline{CE} = \text{High}$ , $V_O = 0.4\text{V}$ $\overline{CE} = \text{High}$ , $V_O = 5.5\text{V}$ $\overline{CE} = \text{Low}$ , $V_O = 0\text{V}$ , High stored	-15		-40	$\mu\text{A}$		
$I_{OS}$	Short circuit <sup>3</sup>						40	$\mu\text{A}$
							-85	mA
<b>Supply current</b>								
$I_{CC}$		$\overline{CE} = \text{High}$ , $V_{CC} = 5.5\text{V}$		90	130	mA		
<b>Capacitance<sup>6</sup></b>								
$C_{IN}$	Input	$\overline{CE} = \text{High}$ , $V_{CC} = 5.0\text{V}$ $V_I = 2.0\text{V}$ $V_O = 2.0\text{V}$			5	10	pF	
$C_{OUT}$	Output							8

## AC ELECTRICAL CHARACTERISTICS $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT	
				Min	Typ <sup>5</sup>	Max		
$t_{AA}$	Access time <sup>4</sup>	185	Output	Address		70	115	ns
		185A			25	55	ns	
		185B			40	90	ns	
$t_{CE}$	Access time <sup>4</sup>	185/185B	Output	Chip Enable		30	50	ns
		185A			15	30	ns	
$t_{CD}$	Disable time	185/185B	Output	Chip Disable		30	50	ns
		185A			15	30	ns	

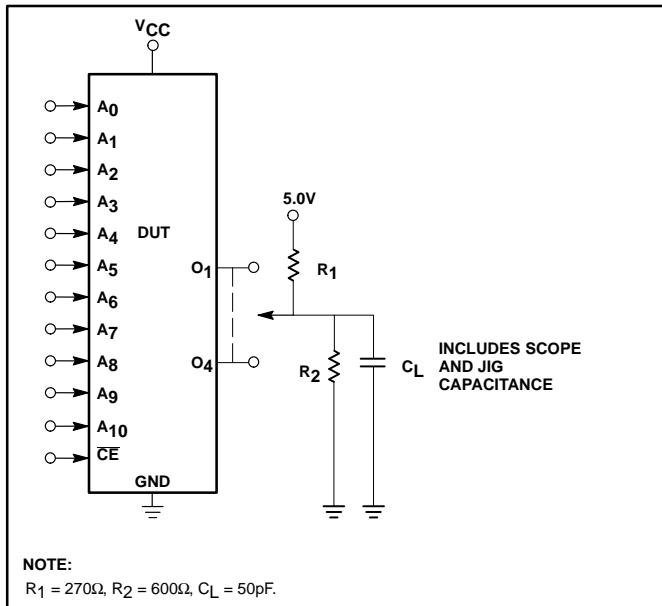
**NOTES:**

1. All voltages are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 $\mu\text{s}$ .
5. Typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = +25^{\circ}\text{C}$ .
6. Guaranteed, but not tested.

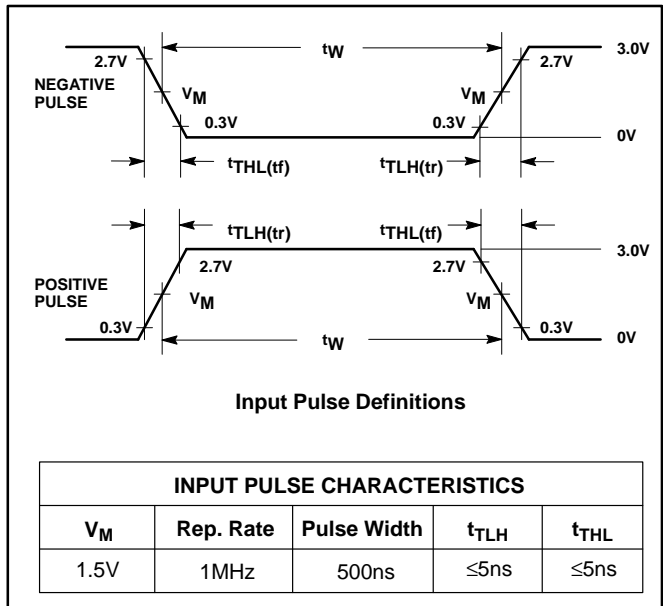
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## TEST LOAD CIRCUITS



## VOLTAGE WAVEFORMS



## TIMING DIAGRAMS

